

CBR Channels on a DQRAP-based HFC Network

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DQRAP Research Group Report 95-2
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ABSTRACT¹

DQRAP (Distributed Queueing Random Access Protocol), is a multiple access protocol that offers a throughput equal to the offered traffic up to a load of one with a lesser delay than any other multiple access protocol. DQRAP utilizes three control minislots and two distributed queues: transmission and collision resolution, to provide this performance for all values of "a", i.e., the size of the network is immaterial. This paper describes: (a) how DQRAP can act as the switching fabric for a distributed ATM switch serving an HFC (hybrid fiber-coax) network; and (b) how CBR (constant bit rate) traffic is supported on our distributed ATM switch, i.e., a DQRAP/ATM switch. Simulation results representing the operation of a DQRAP/ATM switch operating in two modes: (a) The control minislots in dataslots allocated to CBR traffic are utilized in the reservation process; and (b) the control minislot capacity in those slots is allocated to CBR data.

Keywords DQRAP, XDQRAP, ATM, HFC network, distributed ATM switch

1. INTRODUCTION

The utilization of existing cable TV infrastructure and the projected HFC (hybrid fiber-coax) networks for the distribution of both conventional TV signals and the two-way transport of digital information ranging from Internet messages to VOD (video-on-demand) to game playing requires that a MAC (medium access control) method be defined such that the several hundreds to several thousands of homes connected to the system can transmit requests, messages, etc., over what is effectively a single inbound channel. Project IEEE 802.14 has been established to define a standard "Cable TV Protocol" whose main objective will be to provide for timely and efficient use of this inbound channel. 802.14 will address two layers: the physical layer and the MAC layer. This paper describes how DQRAP (Distributed Queueing Random Access Protocol), a contention-based random access protocol not only provides excellent performance as a MAC but also effectively acts as the switching fabric for ATM.

There are two basic methods of allocating the capacity of a MAC layer: (a) a contention-based MAC, and (b) a deterministic MAC. Deterministic MACs, e.g., token bus or token ring, require that an exclusive opportunity to transmit be provided to each station on a regular basis whether or not the station desires to transmit. Even at the expected lower density of several hundreds of homes to a channel this leads to low utilization of the resource so that we conclude that whatever standard is finally

¹ Manuscript prepared August 15, 1995.

selected by Project IEEE 802.14 it will be contention-based at least to the extent of utilizing a contention method to dynamically allocate channels/slots for short or long term use.

DQRAP, developed by Xu and Campbell¹ at the Illinois Institute of Technology, is a remarkable contention-based MAC that achieves up to 100% utilization of available data slots with a delay that approaches that of an ideal M/D/1 queueing system. In addition to the conventional dataslot DQRAP utilizes three control minislots that are randomly accessed by stations to make a reservation for a single dataslot: if successful the station obtains a position on a TQ (distributed global transmission queue) and awaits its turn to transmit. The mechanism just described is a reservation system and as such is probably equal to or superior to any reservation system extant. However DQRAP also has an immediate access feature: when the global transmission queue is empty, ready stations are permitted to transmit their data along with the reservation request. Two or more stations could transmit data simultaneously when the TQ is empty thus causing a collision in the dataslot. But the probability is that the stations transmit requests into different control minislots and the feedback informs all stations how many stations are now on the transmission queue and informs the transmitting stations of their position in that queue. If there is a collision in the control minislots then new reservation requests are blocked while the stations that have collided in a minislot acquire exclusive use of the control minislots to resolve the contention. The DQRAP rules ensure that on average a collision of multiplicity N is resolved in less than N dataslots thus ensuring a throughput of one. Details are available ~~Xu~~ and Campbell.

DQRAP thus provides the immediate access feature of Ethernet® when offered traffic is light but the system moves seamlessly to a reservation system as the traffic load increases, i.e., the global transmission queue is non-empty. The transmission queue, actually a single counter at each station, is always nonempty as the offered traffic approaches 100% so stations do not use the immediate access feature and thus there are no collisions, i.e., all dataslots are utilized. Standard DQRAP is a slotted system thus requires an adaptation layer since most user PDUs offered for transmission are longer than the slot size. The standard ATM Adaptation Layers, AAL 1, 2, 3/4, or 5 (as will be shown later) will do the job.

XDQRAP (Extended DQRAP) developed by Wu and Campbell² is an extension of DQRAP that as well as providing the excellent performance of DQRAP also: (a) supports transmission of variable length frames with a segmenting technique that does not require encapsulation of the individual segments, i.e., an adaptation layer is not required; and (b) supports a priority system¹¹ that allows higher priority transmissions to preempt transmission of lower priority transmissions. The basic difference of XDQRAP is that instead of a station reserving a single dataslot via the control minislots as in DQRAP a single request can be for an arbitrary number of dataslots. This increases the size of the control minislot thus seemingly increasing the overhead but there is a payoff. Using XDQRAP a station reserves the requisite number of slots for a single user PDU thus that PDU can be segmented “naked”, i.e., individual segments may be transmitted without individual encapsulation, i.e., the conventional adaptation layer as used with ATM is not required. Another plus is that since each request to a minislot is in the main for a multiple number of dataslots the DQRAP algorithm for contention resolution now works with only two minislots, thus offsetting to a great degree the increased overhead of the control minislot. The application of XDQRAP to an HFC is described ~~Wu~~ and Campbell.

A second application of XDQRAP to the HFC environment has been proposed to IEEE 802.14 by Koperda et al ³. Their proposal calls for passing the user PDU through a conventional ATM adaptation layer and then utilizing XDQRAP to reserve the required number of slots for the cells carrying that PDU. A benefit to superimposing the adaptation layer on top of XDQRAP, not required as stated above, is that the total number of slots required for all cells of a user PDU can be requested and the cells constituting that PDU will be transmitted sequentially. This reduces the possibility of jitter due to dispersion.

This paper describes a third method of applying DQRAP/XDQRAP to the HFC environment and also describes how CBR service is provided. We propose that what may be termed conventional DQRAP be utilized as the switching fabric for ATM..

2. DQRAP AS A DISTRIBUTED ATM SWITCH

We propose that standard DQRAP (with one minor modification) be utilized as a distributed ATM⁴ switch and that ATM adaptation layers⁴ (AAL) 1-5 be utilized as the interface between a user and the DQRAP/ATM. DQRAP can be described either as a conventional network MAC or a distributed switch. The benefit of the distributed switch analogy is that internal buffers as required in conventional ATM switches are not required in a DQRAP/ATM system -- there is a single distributed global queue that consists of a counter at each station attached to the network. The only modification that need be made to DQRAP is that the immediate access feature is not utilized for the transmission of a cell that is one of a set of cells representing a PDU. Cells that carry self-contained data can utilize the immediate access feature of DQRAP. This is to satisfy the requirement of ATM that cells that constitute a PDU are delivered in order.

Figure 1 illustrates how a user PDU (protocol data unit) is passed to an AAL where it is encapsulated at the CPCS (common part convergence sublayer). After that there is segmentation into ATM cells which are then transmitted via DQRAP dataslots. Fig. 1 shows that after a multiple cell PDU is segmented the ATM cells are "on their own" in contending for the channel.

Three types of traffic are expected on the proposed HFC systems: (a) ABR (available bit rate: conventional computer generated traffic (including interactive game traffic)); (b) VBR (variable bit rate) generally non-real-time packetized video; and (c) CBR (constant bit rate - digitized voice channels). The first, (a), is random or bursty by nature and can sustain extreme variations in interpacket delays. The second type, (b), could consist of packets representing non-real-time video being retrieved for display and thus while there is a limit on the interpacket delay variation a longer overall delay can be tolerated which allows buffering to compensate for reasonable variations in interpacket delay. The third type CBR (constant bit rate) could represent conventional POTS (plain old telephone service) DS0 channels and could be utilized for what technically is VBR traffic. The isochronous packets representing a synchronous channel have severe constraints on how much variation is permitted in interpacket delay.

The major problem facing any communication network including conventional ATM systems is how to support a mixture of the above types of traffic, i.e., guaranteeing a minimum variation in interpacket delay and still achieve overall utilization rates that are economic. There is little problem with

CBR traffic in conventional ATM systems since CBR is allocated “off the top”. The real problem is how best can the remainder of the capacity be utilized? Conventional ATM switching systems address the problem by the use of relatively large buffers at the switching points so that lower priority VBR and ABR cells can be buffered allowing high priority CBR cells to pass through.

ATM does stand for Asynchronous Traffic Method wherein the goal is to achieve efficiencies in network utilization by taking advantage of the statistical fluctuations of offered traffic. It is no longer assumed that the arriving cells in an ATM switch are statistically independent -- almost all traffic starts out as PDUs that are larger than a single cell thus there is some a priori knowledge about cell arrival. Despite the variety of traffic expected in HFC systems and the fact that some guesses can be made about size and arrival rate of PDUs we utilize in this paper a simple model wherein portions of the inbound channel are allocated to CBR traffic and the remainder of the capacity is utilized by individual cells arriving with an exponential interarrival time.

Current ATM networks utilize cell switches at the center of their switching fabric thus provision must be made for buffers at these points. DQRAP moves the switching function to the edge of the fabric along with the queues. It is both reasonable and provides the severest test of a MAC functioning as an ATM switch if all the non-CBR traffic consists of single cells with an exponential interarrival pattern. The model used here could be one where our HFC network is providing conventional POTS service via CBR VCIs using AAL 1 and the remainder of the capacity is used to transmit requests for POTS channels, Internet traffic, game playing, etc. The single cell traffic could also represent voice channels that are virtual, i.e., carrying a cell only when sound is present. Such a scheme supported by DQRAP is described by Lin and Campbell.

3. CONSTANT BIT RATE STREAMS IN A DQRAP/ATM SWITCH

A CBR VCI (virtual channel identifier) or stream is requested in the conventional manner by the user transmitting a request to the network manager for a stream that guarantees the required bandwidth. If the resource is available an acknowledgment is returned and the user can begin transmitting at the requested rate. In the conventional ATM world the network manager subtracts the bandwidth allocated from that available and then trusts that even with the “overbooking” of VBR, ABR, and UBR channels there will be adequate capacity at intermediate switches along the virtual path such that the cells utilizing the CBR stream will not be subject to interpacket delays that exceed guaranteed maximums.

In DQRAP/ATM the request for a guaranteed bandwidth stream results in “ownership” being granted to a dataslot on a repeating basis. For instance if the channel capacity is 4000 dataslots per second, each capable of supporting a single ATM cell of 48 bytes payload then the net bit rate is 1.536 Mbps (net DS1). A station requesting bandwidth corresponding to a DS0 channel would be allocated every 24th slot. In a conventional ATM system even though CBR channels are “off the top” the granting of too much capacity to VCIs carrying ABR and VBR traffic could jeopardize the timely delivery of CBR cells. In DQRAP/ATM once allocated the CBR channel need not be further considered, i.e., serious overloading of the remaining channels has no effect on the operation of the CBR channel. For all practical purposes the station requesting a CBR channel is allocated the equivalent of an STM (synchronous transfer mode) channel. In our simulations we present the delay characteristics

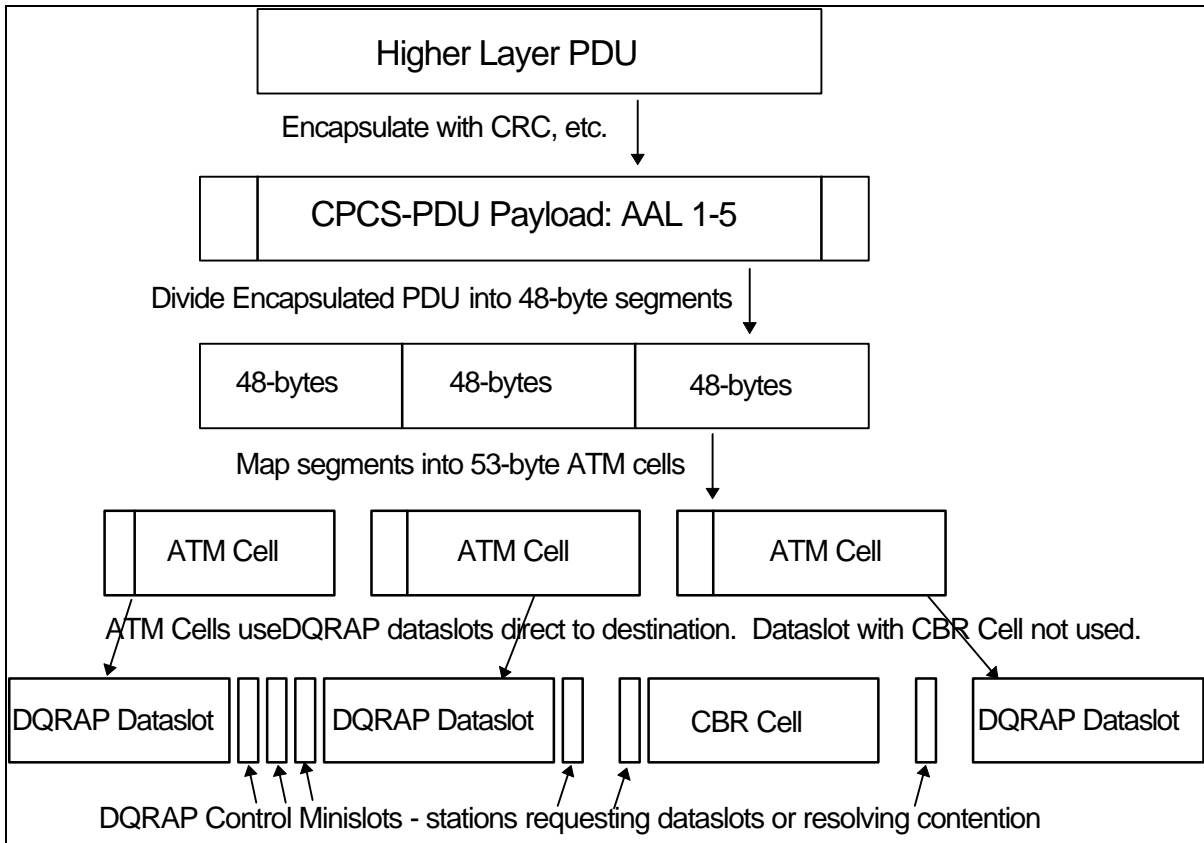


Figure1 DQRAP as the Switching Fabric for ATM

for only the random traffic since the intercell delay for the CBR cells will be constant to the bit resolution of the carrier. Furthermore we assume the non-CBR traffic consists solely of offered traffic that consists of single cells and whose arrival pattern is exponentially distributed. This type of traffic load has been used for analysis and simulation since the development of the Aloha⁶ family of protocols and is the most stressful test to which a contention MAC can be subjected. Figure 2 presents the throughput of many of the well known MACs along with DQRAP and the curve representing the throughput of an idealized MAC, i.e., one that equaled the performance of an M/D/1 queue. Note that DQRAP approaches the ideal.

4. SIMULATION RESULTS

Two simulation studies were conducted. Tables 1 (a-j) present the delay encountered by single ATM cells arriving with an exponential interarrival distribution such that total offered load is 0.95 of capacity including a CBR traffic component that ranges from 0.0 to 0.9 in increments of 0.1. Tables 2 (a-j) present simulation results when the CMSs in slots allocated to CBR traffic are not used for reservation and contention resolving but instead the capacity utilized by the CMS is utilized by the CBR channel. This is discussed in section 4.1.

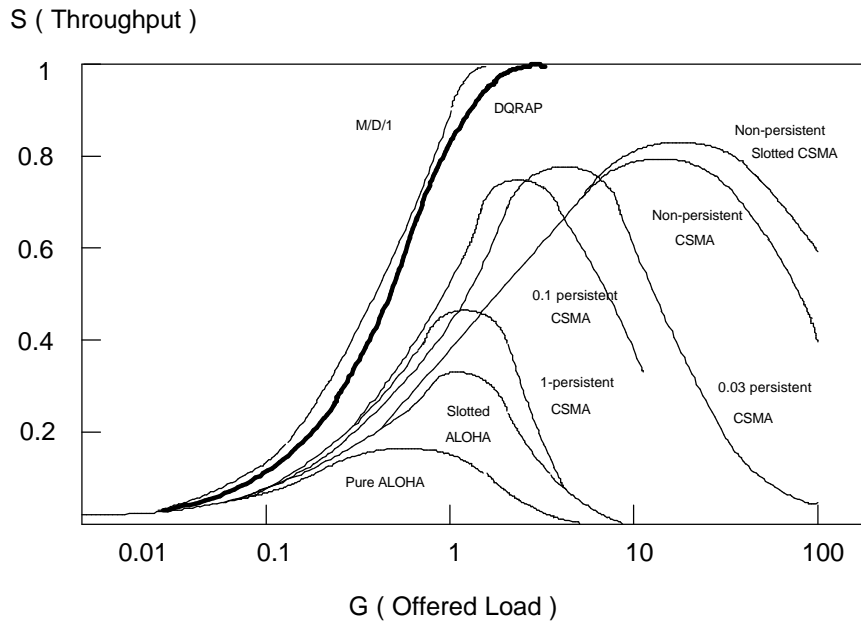


Figure 2. Comparative Throughputs of Well Known MACs

We first look at the results in Table 1(a). In this instance the total offered traffic consists of single cells arriving with an exponential interarrival distribution; there is no CBR traffic. Note that at a total offered load of 0.95 or 95% of capacity the average delay of a cell is 13.33 dataslots. Assuming the cell rate discussed in Section 3, i.e., 4000 cells per second, this indicates a typical access delay of $1/4000 * 13.33 = 3.3$ milliseconds. It is well to remember that while the theoretical upper limits of the MACs listed in Figure 2 indicate in some instances throughputs in the 50% plus range in practice the practical average traffic limit is 20% - 30%. Thus throughput at 95% offered load with a delay of 13.3 slots is unique. We also present the maximum delay encountered at the various loads during the simulation runs of 1,000,000 slots. At 0.95 offered load this is 87.30 slots or in real terms approximately 22 ms for our 1.536 Mbps HFC.

The theoretical delay of DQRAP has been studied by Zhang and Campbell⁷ and is presented in Equation 1. $E_{DFI}[t]$ is the theoretical delay for a system where feedback is received at the end of the current dataslot, i.e., the slot size is at least twice the propagation delay of the network.

$$E_{DFI}[t] = \frac{(3 - 2\lambda)(\ln 1 / (1 - e^{-\lambda/M}) - \lambda) + 2(1 - \lambda)}{2(1 - \lambda)(\ln 1 / (1 - e^{-\lambda/M}) - \lambda)} +$$

$$\left((1 + \lambda \left(1 - \frac{(1 - \lambda_{tq})(1 - e^{-\lambda})}{1 + (1 - e^{-\lambda})}\right)) \right) \frac{(1 - \lambda)(1 - e^{-\lambda})}{1 + (1 - e^{-\lambda})} \quad (\text{Eq. 1})$$

where λ = input rate

M = number of minislots

λ_{tq} = input rate to transmission queue - equal to λ when $M \geq 3$.

Equation 1 represents the conditions of Table 1(a) where CBR load is zero. The formula predicts a delay of 2.92 slots at $\lambda = 0.5$, 8.29 slots at $\lambda = 0.90$, and 13.86 slots at $\lambda = 0.95$. This compares well with the values of 2.98, 8.40, and 13.33 slots respectively in Table 1(a) for similar loading. The delay of an ideal M/D/1 system at $\lambda = 0.95$ is 11.0 dataslots thus we see the close to ideal performance of DQRAP.

Table 1(f) represents the results of a series of simulations where the CBR traffic constitutes 0.5 of the available capacity. This could represent 12 DS0 connections. The maximum delay for the random portion of the traffic at a total offered load, including CBR, of 0.95 is 11.88 slots. This is a shorter access time than for the situation where all traffic is random. Inspection of the final column in Table 1 shows that the access delay for the random traffic decreases as the portion of CBR traffic increases. At the point where 90% of the load is CBR (Table 1(j)) the access delay has been reduced by over two slots from the delay in Table 1(a).

The decreasing delay as load increases is explained as follows: the DQRAP rules state that three control minislots are sufficient to ensure that 100% of the dataslots will be utilized. When the CBR traffic is at 0.5 of total capacity that means that 50% of the available dataslots have been “removed from service” with respect to random access. The minislots available in each of these dataslots are now available, along with all other minislots, to stations contending for the remaining 50% of the dataslots. Contention in the minislots is reduced and thus access delay is reduced.

4.1 Utilizing CBR minislots for data

We observe that allocating a CBR channel increases the number of minislots available for the random traffic thus reducing the access delay for that traffic. The complementary situation is that when a slot is allocated to a CBR stream the stream is allowed to utilize the entire slot including the capacity allocated for the three minislots. Figure 3 illustrates the action. The theory of operation of DQRAP⁷ tells us that there is still sufficient minislots to provide 100% utilization of the dataslots. There is

obviously a longer average delay till a minislot can be accessed so what is the impact on delay for the random traffic?

Table 2 presents the results of simulations where the minislot capacity in CBR slots has been allocated to the CBR channel. At 50% CBR traffic (Table 2(f) the average delay for the random traffic is 15.63 slots, an increase of slightly more than two slots over the zero CBR case. In practical terms this is still under 4 ms. At the maximum CBR traffic of 0.90 (Table 2(j)) the access delay for the random traffic is 20.76 slots or approximately 5 ms. When 0.9 of capacity is allocated to CBR channels contending stations cannot access approximately 21 minislots out of a frame length of 24. However actual average access delay in our sample system is still just approximately 5 ms.

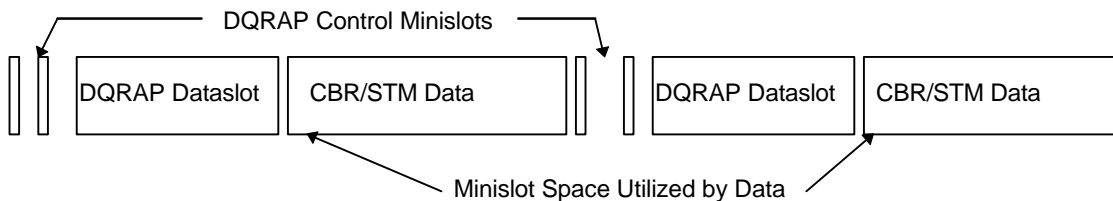


Figure 3 Utilizing DQRAP Minislot Capacity for Data

5. PRACTICAL CONSIDERATIONS

The theoretical performance claims for DQRAP are not in dispute. As with all new technology there is a concern about whether the theory can be reduced to practice. With respect to DQRAP the main concern is with the overhead of the control minislots. Certainly if each minislot consumed the same bandwidth as a dataslot then DQRAP would not be viable as the switching fabric for ATM or for any other application.

But the minislots need not consume an inordinate amount of capacity -- a minislot does not have to carry classical data -- it need only consist of enough signal energy such that a receiver can differentiate between (a) absence of a signal, (ii) presence of a single signal, and (iii) presence of two or more signals indicating a collision. In DSx or other circuits where synchronization to the bit level is provided the control minislots in DQRAP can consist of two bits each for a total of less than one byte thus incurring an overhead of $6/(424+6) = 1.4\%$ when used with ATM cells. The problem is that in an RF environment detection of a collision is a non-trivial task since colliding transmissions are non-coherent. A method described by Campbell and Xu⁸ overcomes this problem in that each station is assigned a unique pattern that is transmitted by that station in a minislot. The arrival of a single pattern identifies the station (not actually necessary in the protocol) and arrival of two or more simultaneous patterns is easily detected as a collision by the overlapping of the unique patterns. The reception and identifying of the content of the minislots is further simplified by the fact that the system is synchronous in that the receiver is aware to the precision of the overall system when a minislot is due to arrive and the duration to the bit time of the minislot.

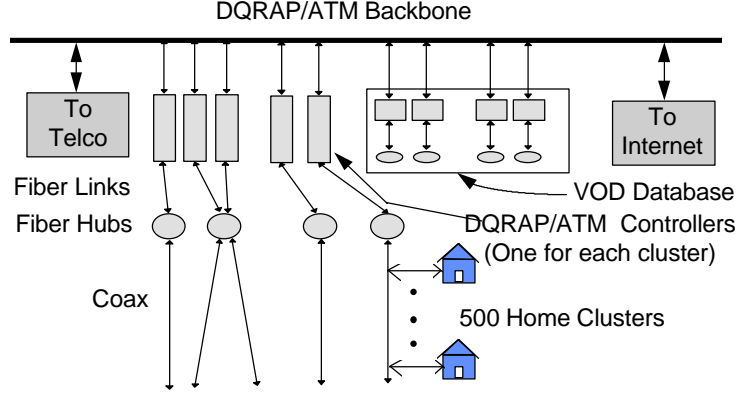


Figure 4. HFC Network Supported by DQRAP/ATM Switch

Either conventional detection techniques or analysis of the minislot using DSP technology will do the job. It is estimated that the equivalent of 16-20 bit times for each minislot will be sufficient leading to an overhead factor of approximately 10% - 12%. XDQRAP requires a length field in the minislot thus a self contained transmission for the minislot, i.e., preamble, sync, data field, and frame check sequence can be used^{3,4}. The extra overhead per minislot in XDQRAP is partly offset by the requirement of but two minislots in XDQRAP. The collision detection process is also simplified.

Another practical consideration is the radius of the HFC network. A cell size of 250 microseconds (4000 cells per second) means that the network can have a radius of up to approximately 20 km without requiring interleaving of the cells. But beyond this radius or as the channel speed increases dataslots must be organized into frames whose length is at least twice the radius of the network in bits.⁹ Tables 1 and 2 assume an interleaving factor of 1. However DQRAP is amenable to interleaving and the delay can be calculated by using Equations 2 and 3 as shown by Zhang¹⁰. Equation 3 represents the delay when a global TQ is used, i.e., all stations contend in separate collision resolution queues, one for each slot in the frame, but then join a common global queue.

$$E[t_{rq}] = \frac{1}{\ln 1 / (1 - e^{-(\lambda/M)}) - \lambda} \quad (\text{Eq. 2})$$

$$E_{DFGn}[t] = E_{DF1}[t] + (n-1) E[t_{rq}] \quad (\text{Eq. 3})$$

where $E[t_{rq}]$ is the expected delay in the collision resolution queue.
 n is the interleaving factor.

The overall delay as shown in Eq. 3 is the delay of a single slot system plus the collision resolution delay, $E[t_{rq}]$, multiplied by a constant associated with the interleaving factor. $E[t_{rq}]$ ranges in value from 0 at $\lambda = 0$ up to 2.84 at $\lambda = 0.95$. The delay for offered load of 0.95 in a system with an interleaving factor of 10 is 39.42 slots. If our sample system of 4000 cells per second was increased in

speed to 40,000 cells per second then the delay would be 39.42×25 microseconds ≈ 1 ms. This is a considerable reduction in the delay from the approximate 3 ms for the 4000 cells/s system and is due to the decreased slot size -- we see that delay is a function of the slot size. Of course if our 4000 cells/s system required an interleaving factor of 10 because of increased propagation delay then the delay would be approximately 10 ms. Overall the global queueing system of DQRAP provides excellent performance over any distance however we cannot overcome plain old propagation delay in getting feedback back to a station.

6. CONCLUSIONS

6.1 General observation

A guess is that there are probably some 20 MACs now officially or unofficial being considered by IEEE 802.14. Many of these MACs will have been developed to address the specific conditions of an HFC, i.e., distance, capacity, topology, and expected traffic (but surely at this stage of the game estimating future traffic in this environment requires considerable courage). DQRAP is however a generic MAC suitable for all distances, bit rates, and topologies. Figure 4 illustrates a typical HFC network. Note that the DQRAP/ATM controllers serving the clusters of homes are connected to what is described as a DQRAP/ATM backbone. The significance is that the DQRAP/ATM MAC described for the fiber-coax portion of the network is also applicable to the backbone function; something that is commonly delegated to other MACs, i.e., FDDI, SONET, or other types of switches. Furthermore the backbone shown here can be connected to WANs at all DSx speeds that could also utilize DQRAP to move data with the same throughput and delay characteristics demonstrated for our HFC network. DQRAP/ATM can be regarded as a generic solution to providing data communications over LANs, MANs, and WANs, as well as our HFC network

6.2 Two specific points

(i) A method, DQRAP/ATM, is proposed as the switching fabric for an HFC network.

DQRAP/ATM. is the third method proposed that utilizes DQRAP as the basis of method presented for utilizing DQRAP at the MAC layer in an HFC environment. The other two are XDQRAP and XDQRAP/ATM. A brief review of the three methods

XDQRAP has the advantage that SAR does not require that the individual segments be encapsulated -- they can be transmitted as is. If enough information is transmitted in the CMS then XDQRAP does not require encapsulation of the user PDU for transmission - the operation operates as what may be described as a "pure" switch where the data is transported without any addition. There is a tradeoff between overhead and complexity in deciding where to put the control and addressing information: in the control minislot or in an encapsulated user PDU. Further research is required to determine the optimal strategy but early results indicate that encapsulation of the user PDU with an IEEE 802-like frame and minimization of the minislot looks promising.

XDQRAP/ATM works as does XDQRAP with the exception that the ATM AAL process is carried out above the XDQRAP layer. The remainder of the process is the same as XDQRAP except that the segments transmitted in the XDQRAP dataslots contain five bytes header of the ATM cell. This overhead is redundant from an operational point of view but the standard ATM interface is provided. In conventional ATM the cells constituting a user PDU are “on their own” when going through the system. In XDQRAP/ATM a reservation is made for the complete set of cells and they thus they are switched as a set. This lowers total time foreassembly reducing the potential fojitter.

DQRAP/ATM provides the standard ATM interface but the ATM cells constituting a user PDU contend for access to the network on an individual basis. As shown in Tables 1 and 2 the average performance is excellent but further research is required to determine whether in practical terms the quality of transmission is impaired.

(ii) A description is presented of how CBR channels are supported in DQRAP/ATM.

There has been concern that DQRAP pays a penalty in minislots. The authors do not concur since we believe that a minislot overhead of even 15%- 20% still leaves DQRAP very competitive. However if it is a concern we haave demonstrated that the minislot capacity can be recovered not only in CBR channels but also even with “trains” of cells. These steps result in overall utilization rate that few MACs can match.

DQRAP/ATM must be given serious consideration as the MAC for the HFC environment.

TABLE 1 - Mixed CBR and Random Traffic CMSs Utilized

Table 1(a) CBR Traffic = 0.0										
Total Load	0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load	0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Avg. Delay	1.71	1.97	2.25	2.58	2.98	3.48	4.20	5.36	8.40	13.33
Max. Delay	11.33	16.45	16.90	18.94	23.38	27.37	29.52	40.53	85.22	87.30
Table 1(b) CBR Traffic = 0.1										
Total Load		0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load		0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.85
Avg. Delay		1.83	2.11	2.43	2.82	3.31	3.97	5.13	7.93	13.30
Max. Delay		14.48	18.79	16.99	19.78	28.02	25.61	38.72	55.64	97.48
Table 1(c) CBR Traffic = 0.2										
Total Load			0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load			0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.75
Avg. Delay			1.95	2.26	2.62	3.10	3.76	4.81	7.70	12.92
Max. Delay			10.99	16.58	16.95	19.16	26.97	31.24	44.94	89.37
Table 1(d) CBR Traffic = 0.3										
Total Load				0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load				0.10	0.20	0.30	0.40	0.50	0.60	0.650
Avg. Delay				2.07	2.43	2.87	3.53	4.61	7.35	12.47
Max. Delay				11.45	15.63	19.54	23.18	34.06	45.88	74.99
Table 1(e) CBR Traffic = 0.4										
Total Load					0.50	0.60	0.70	0.80	0.90	0.95
Random Load					0.10	0.20	0.30	0.40	0.50	0.55
Avg. Delay					2.23	2.68	3.29	4.39	7.09	12.12
Max. Delay					12.52	25.30	20.70	42.49	47.83	90.89
Table 1(f) CBR Traffic = 0.5										
Total Load						0.60	0.70	0.80	0.90	0.95
Random Load						0.10	0.20	0.30	0.40	0.45
Avg. Delay						2.41	3.03	4.06	6.85	11.88
Max. Delay						14.77	19.86	28.54	57.96	106.18
Table 1(g) CBR Traffic = 0.6										
Total Load							0.70	0.80	0.90	0.95
Random Load							0.10	0.20	0.30	0.35
Avg. Delay							2.88	3.93	6.58	11.98
Max. Delay							19.40	27.59	51.26	79.51
Table 1(h) CBR Traffic = 0.7										
Total Load								0.80	0.90	0.95
Random Load								0.10	0.20	0.25
Avg. Delay								3.68	6.45	11.26
Max. Delay								23.67	57.79	83.79
Table 1(i) CBR Traffic = 0.8										
Total Load									0.90	0.95
Random Load									0.10	0.20
Avg. Delay									6.17	11.55
Max. Delay									60.81	96.88
Table 1(j) CBR Traffic = 0.9										
Total Load										0.95
Random Load										0.05
Avg. Delay										11.18
Max. Delay										120.63

TABLE 2 - Mixed CBR and Random Traffic CMSs Not Utilized

Table 2(a) CBR Traffic = 0.0										
Total Load	0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load	0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Avg. Delay	1.71	1.97	2.25	2.58	2.98	3.48	4.20	5.36	8.40	13.33
Max. Delay	11.33	16.45	16.90	18.94	23.38	27.37	29.52	40.53	85.22	87.30
Table 2(b) CBR Traffic = 0.1										
Total Load		0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load		0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.85
Avg. Delay		1.88	2.20	2.58	3.01	3.56	4.30	5.55	8.60	14.25
Max. Delay		16.22	14.28	19.60	20.78	41.89	37.58	42.19	60.88	117.92
Table 2(c) CBR Traffic = 0.2										
Total Load			0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load			0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.75
Avg. Delay			2.05	2.47	2.96	3.56	4.38	5.66	8.93	14.60
Max. Delay			13.60	18.46	20.92	30.36	35.31	39.94	69.85	109.61
Table 2(d) CBR Traffic = 0.3										
Total Load				0.40	0.50	0.60	0.70	0.80	0.90	0.95
Random Load				0.10	0.20	0.30	0.40	0.50	0.60	0.650
Avg. Delay				2.27	2.84	3.51	4.42	5.81	9.11	14.81
Max. Delay				14.98	20.55	24.61	36.13	47.23	74.40	92.95
Table 2(e) CBR Traffic = 0.4										
Total Load					0.50	0.60	0.70	0.80	0.90	0.95
Random Load					0.10	0.20	0.30	0.40	0.50	0.55
Avg. Delay					2.54	3.36	4.38	5.93	9.44	15.09
Max. Delay					19.34	27.68	30.33	46.91	76.40	111.86
Table 2(f) CBR Traffic = 0.5										
Total Load						0.60	0.70	0.80	0.90	0.95
Random Load						0.10	0.20	0.30	0.40	0.45
Avg. Delay						2.92	4.17	5.92	9.77	15.63
Max. Delay						24.39	41.36	43.85	115.33	122.78
Table 2(g) CBR Traffic = 0.6										
Total Load							0.70	0.80	0.90	0.95
Random Load							0.10	0.20	0.30	0.35
Avg. Delay							3.80	6.04	10.18	16.82
Max. Delay							29.61	48.50	106.93	130.04
Table 2(h) CBR Traffic = 0.7										
Total Load								0.80	0.90	0.95
Random Load								0.10	0.20	0.25
Avg. Delay								5.58	10.84	17.51
Max. Delay								43.97	96.39	140.02
Table 2(i) CBR Traffic = 0.8										
Total Load									0.90	0.95
Random Load									0.10	0.20
Avg. Delay									10.84	19.67
Max. Delay									84.13	148.51
Table 2(j) CBR Traffic = 0.9										
Total Load										0.95
Random Load										0.05
Avg. Delay										20.76
Max. Delay										167.26

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